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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,276	02/09/2004	Tomoo Kimura	2004_0156A	1091

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,276	KIMURA ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7-9,11,12,14,18-20 and 22* is/are rejected.

7)☒ Claim(s) *2,4-6,10,13,15-17 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/04*. 7-19-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/773,279 filed on 2/9/2004. Claims 1-22 remain pending in the application.

Specification

2. The claiming foreign priority information is missing on first sentence of the application. Appropriate correction is required.

Claim Objection

3. Claim 21, line 1, "claim 12" should be –claim 20--. Applicant is requested to properly correct claim dependency.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 10 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It appears that the limitation following the "wherein" clause is ambiguous because it is not clear where a new flip-flop to be inserted. As a result, the claim appears to be missing step.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3, 7-9, 11-12, 14, 18-20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Dai et al. (5,452,239).

8. As to claim 1, Dai et al. teach a logic optimizing method (at least see Fig. 13, timing optimization, optimized netlist; Fig. 14, optimize 104; Fig. 15, optimize and partition; Fig. 30 logic optimization; Fig. 80 optimizer, clusters; Fig. 81A optimizer, clusters; Fig. 82 partitioning and clustering) comprising clustering logic circuit to obtain primary clusters (Fig. 80 clusters; Fig. 81A cluster steps; Fig. 82 clustering; Fig. 79; Fig. 81B, 81C); inserting a flip-flop to a cluster whose cluster length exceeds predetermined cluster length, the cluster being one of the primary clusters obtained in said clustering (col. 53 lines 10-67; col. 54 line 1-11; Fig. 79, 81B-C); and re-clustering the flip-flop inserted clusters to obtain secondary clusters (Fig. 80, subsequent clusters; Fig. 81A subsequent clusters; Fig. 81D newly formed cluster). In addition, Dai et al. teach a delay insertion module in Fig. 30, where delay elements (buffers, gates or flip-flops) are appropriately inserted to correct delay problems in a circuit design.

9. As to claim 9, remarks set forth in rejecting claim 1 equally apply because of substantially same claim limitations. In addition, these clusters as taught by Dai et al. are allotted to variable logic element of a logic emulation device within a system 10 (Fig. 1, emulation array 16, logic chips 18).

10. As to claim 12, remarks set forth in rejecting claim 1 equally apply because of substantially same claim limitations. In addition, Dai et al. teach clustering unit at least

in Fig. 80, 81A, 82; a circuit dividing unit or partitioner in Figs. 14 & 15 item 108; partitioner in Figs. 81A, 82).

11. As to claim 20, remarks set forth in rejecting claim 1 and 12 equally apply because of substantially same claim limitations. In addition. Dai et al. teach clustering is based on gate count that is a number of gates to be fitted in a module (col. 53 lines 10-37).

12. As to claims 3 and 14, remarks set forth in rejecting claim 20 equally apply in rejecting claim 3 because of substantially same claim limitations. In addition, these clusters as taught by Dai et al. are allotted to variable logic element of a logic emulation device within a system 10 (Fig. 1, emulation array 16, logic chips 18). Clustering and re-clustering (subsequent clustering) are shown in Figs. 80 and 81A).

13. As to claims 7-8 and 18-19, Dai et al. teach cluster length is expressed in terms of a number cascading circuit stages and in terms of a signal propagation time (at least see col. 53, lines 10-67; Fig. 81B-D).

As to claims 11 and 22, Dai et al. teach substantially the same claim limitations. Dai et al. teach a logic optimizing method and device (at least see Fig. 13, timing optimization, optimized netlist; Fig. 14, optimize 104; Fig. 15, optimize and partition; Fig. 30 logic optimization; Fig. 80 optimizer, clusters; Fig. 81A optimizer, clusters; Fig. 82 partitioning and clustering) comprising clustering logic circuit to obtain primary clusters (Fig. 80 clusters; Fig. 81A cluster steps; Fig. 82 clustering; Fig. 79; Fig. 81B, 81C). The partitioning provides modules. Each of the modules has number of operational elements (gate count). The gate count is determined by calculating a number of

operational elements or gates to be included in a cluster or module. Dai et al. teach delay insertion module that is used to insert delay elements (buffers, gates or flip-flops) to a module to correct delay problems (col. 53 lines 10-67; col. 54 lines 1-11; Fig. 79,

Allowable Subject Matter

14. Claims 2, 13; 4-6, 15-17; and 10 & 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and to rewritten to overcome the rejection under 35 U.S.C. 112, second paragraph above (claims .

15. The prior art of record does not teach or fairly suggest measuring cluster length of each primary clusters; selecting step; and inserting and re-clustering step; inserting a new flip-flop after re-clustering to a cluster, said new flip-flop to be inserted having higher operation clock frequency than that of a flip-flip already included in a cluster to which the new flip-flop is to be inserted.

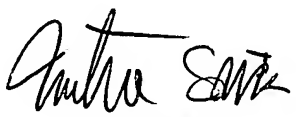
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER